In the Claims:

1. (Original) An apparatus comprising:

a check bit encoder circuit coupled to receive a data block, wherein the check bit encoder circuit is configured to generate a corresponding encoded data block comprising the data block, a first plurality of check bits, and a second plurality of check bits; and

a check/correct circuit coupled to receive an encoded data block, the check/correct circuit configured to detect an error in data from one of a plurality of components and correct the error using the first plurality of check bits, the second plurality of check bits, and the data block within the encoded data block;

wherein the encoded data block is logically arranged as an array of R rows and N columns, wherein R and N are positive integers, and wherein each of the N columns comprises data bits from a respective one of the plurality of components, and wherein the first plurality of check bits form a first column of the array, and wherein each of the first plurality of check bits covers a row of the array, and wherein the second plurality of check bits form a second column of the array and are defined to cover bits in the array according to a plurality of check vectors, each of the plurality of check vectors corresponding to a different bit in the array, and each of the plurality of check vectors is an element of a Galois Field ($GF(2^R)$), and wherein the plurality of check vectors are derived from a plurality of unique elements of $GF(2^R)$, each of the plurality of unique elements corresponding to a different column of the array, and wherein the check vector in row X of the column is the product, in $GF(2^R)$ of the unique element for that column and $alpha^X$, wherein alpha is a primitive element of $GF(2^R)$.

2. (Original) The apparatus as recited in claim 1 wherein a first element of the plurality of unique elements corresponding to the first column is all zeros, whereby the first

column is not covered by the second plurality of check bits.

3. (Original) The apparatus as recited in claim 2 wherein a second element of the plurality of unique elements corresponding to the second column is all zeros except for a one in the least significant position, and wherein the position of the one in each of the plurality of check vectors corresponding to the second column defines the location in the second column that stores the corresponding one of the plurality of check bits.

4. (Original) The apparatus as recited in claim 1 wherein the plurality of unique elements are selected to provide double bit error detection prior to the apparatus identifying a failure of one of the plurality of components.

5. (Original) The apparatus as recited in claim 4 wherein the plurality of unique elements are selected to satisfy the following, where check_vector(r_x, c_y) is the check vector assigned to the bit at row x, column y of the array and XOR is bitwise exclusive OR: for any set of 2 distinct rows r_1 and r_2 and any set of 3 distinct columns c_1, c_2, and c_3, check_vector(r_1, c_1) XOR check_vector(r_2, c_2) XOR check_vector(r_1, c_3) XOR check_vector(r_2, c_3) is not equal to zero.

6. (Original) The apparatus as recited in claim 4 wherein the plurality of unique elements are selected to satisfy the following, wherein each of the plurality of unique elements is denoted UE[column to which the unique element corresponds]: for any integer W between 0 and R-1 (inclusive), for any integers i, j, and k between 0 and N-1 (inclusive), where i is not equal to j and i is not equal to k, and j is not equal to k, UE[i] XOR UE[j] is not equal to the product, in GF(2^R), of UE[i] XOR UE[k] and alpha^W.

7. (Original) The apparatus as recited in claim 1 wherein the plurality of unique elements are selected to provide single bit error correction subsequent to the apparatus identifying a failure of one of the plurality of components.

8. (Original) The apparatus as recited in claim 7 wherein the plurality of unique

elements are selected to satisfy the following, where check_vector(r_x, c_y) is the check vector assigned to the bit at row x, column y of the array and XOR is bitwise exclusive OR: for any set of 2 distinct rows r_1 and r_2 and any set of 3 distinct columns c_1, c_2, and c_3, check_vector(r_1, c_1) XOR check_vector(r_2, c_2) XOR check_vector(r_1, c_3) XOR check_vector(r_2, c_3) is not equal to zero.

9. (Original) The apparatus as recited in claim 7 wherein the plurality of unique elements are selected to satisfy the following, wherein each of the plurality of unique elements is denoted UE[column to which the unique element corresponds]: for any integer W between 0 and R-1 (inclusive), for any integers i, j, and k between 0 and N-1 (inclusive), where i is not equal to j and i is not equal to k, and j is not equal to k, UE[i] XOR UE[j] is not equal to the product, in GF(2^R), of UE[i] XOR UE[k] and alpha^W.

10. (Original) A memory controller comprising the apparatus as recited in claim 1, wherein the plurality of components are a plurality of memory devices.

11. (Original) A transmission system comprising the apparatus as recited in claim 1 wherein the plurality of components are a plurality of paths on a transmission medium in the system.

12. (Original) The transmission system as recited in claim 11 further comprising a source coupled to the plurality of paths to transmit encoded data blocks and a destination coupled to the plurality of paths to receive encoded data blocks, wherein the source comprises the check bit encoder circuit and the destination comprises the check/correct circuit.

13-17. (Cancelled)

18. (Original) A computer system comprising:

at least one processor;

at least one memory comprising a plurality of memory devices; and

at least one memory controller coupled to the processor and to the memory, wherein the memory controller is coupled to receive data blocks from the processor for storage in the memory and coupled to provide data blocks read from the memory to the processor, and wherein the memory controller is configured to generate a corresponding encoded data block in response to receive a data block from the processor, the encoded data block including a first plurality of check bits, a second plurality of check bits, and the data block, and wherein the memory controller is configured to detect an error in data from one of the plurality of memory devices and correct the error using the first plurality of check bits, the second plurality of check bits, and the data block within the encoded data block;

wherein the encoded data block is logically arranged as an array of R rows and N columns, wherein R and N are positive integers, and wherein each of the N columns comprises data bits from a respective one of the plurality of memory devices, and wherein the first plurality of check bits form a first column of the array, and wherein each of the first plurality of check bits covers a row of the array, and wherein the second plurality of check bits form a second column of the array and are defined to cover bits in the array according to a plurality of check vectors, each of the plurality of check vectors corresponding to a different bit in the array, and each of the plurality of check vectors is an element of a Galois Field ($GF(2^R)$), and wherein the plurality of check vectors are derived from a plurality of unique elements of $GF(2^R)$, each of the plurality of unique elements corresponding to a different column of the array, and wherein the check vector in row X of the column is the product, in $GF(2^R)$ of the unique element for that column and alpha^X, wherein alpha is a primitive element of $GF(2^R)$.

19. (Original) The computer system as recited in claim 18 wherein a first element of the plurality of unique elements corresponding to the first column is all zeros, whereby the

first column is not covered by the second plurality of check bits.

20. (Original) The computer system as recited in claim 19 wherein a second element of the plurality of unique elements corresponding to the second column is all zeros except for a one in the least significant position, and wherein the position of the one in each of the plurality of check vectors corresponding to the second column defines the location in the second column that stores the corresponding one of the plurality of check bits.

21. (Original) The computer system as recited in claim 18 wherein the plurality of unique elements are selected to provide double bit error detection prior to the memory controller identifying a failure of one of the plurality of memory devices.

22. (Original) The computer system as recited in claim 18 wherein the plurality of unique elements are selected to provide single bit error correction subsequent to the memory controller identifying a failure of one of the plurality of memory devices.

23. (New) A method comprising:

receiving an encoded data block comprising a data block, a first plurality of check bits, and a second plurality of check bits;

detecting an error in data of the encoded data block that is from one of a plurality of components; and

correcting the error using the first plurality of check bits, the second plurality of check bits, and the data block within the encoded data block; wherein the encoded data block is logically arranged as an array of R rows and N columns, wherein R and N are positive integers, and wherein each of the N columns comprises data bits from a respective one of the plurality of components, and wherein the first plurality of check bits form a first column of the array, and wherein each of the first plurality of check bits

covers a row of the array, and wherein the second plurality of check bits form a second column of the array and are defined to cover bits in the array according to a plurality of check vectors, each of the plurality of check vectors corresponding to a different bit in the array, and each of the plurality of check vectors is an element of a Galois Field ($GF(2^R)$), and wherein the plurality of check vectors are derived from a plurality of unique elements of $GF(2^R)$, each of the plurality of unique elements corresponding to a different column of the array, and wherein the check vector in row X of the column is the product, in $GF(2^R)$ of the unique element for that column and $alpha^X$, wherein alpha is a primitive element of $GF(2^R)$.

24. (New) The method as recited in claim 23 wherein a first element of the plurality of unique elements corresponding to the first column is all zeros, whereby the first column is not covered by the second plurality of check bits.

25. (New) The method as recited in claim 24 wherein a second element of the plurality of unique elements corresponding to the second column is all zeros except for a one in the least significant position, and wherein the position of the one in each of the plurality of check vectors corresponding to the second column defines the location in the second column that stores the corresponding one of the plurality of check bits.

26. (New) The method as recited in claim 23 wherein the plurality of unique elements are selected to provide double bit error detection prior to identifying a failure of one of the plurality of components.

27. (New) The method as recited in claim 23 wherein the plurality of unique elements are selected to provide single bit error correction subsequent to identifying a failure of one of the plurality of components.